a $Si_{1-x}Ge_x$ channel region, having a germanium molar fraction of x, and formed in the substrate, underneath [and adjoining] a silicon dioxide (SiO_2) gate oxide and between a source region and a drain region;

wherein x is less than or equal to 0.6, and wherein the $Si_{1-x}Ge_x$ channel region forms a $Si_{1-x}Ge_x/SiO_2$ gate oxide interface.

[wherein the $Si_{1-x}Ge_x$ channel region has a channel length less than 7μm.]

25. (Four times amended) A p-channel metal-oxide-semiconductor transistor formed on a silicon substrate, comprising:

a $Si_{1-x}Ge_x$ channel region, having a germanium molar fraction of x, and formed in the substrate, underneath a silicon dioxide (SiO_2) gate oxide and between a source region and a drain region [without a silicon layer interposed between the $Si_{1-x}Ge_x$ channel region and the gate oxide;], wherein x is less than or equal to 0.6, and wherein the $Si_{1-x}Ge_x$ channel region forms a $Si_{1-x}Ge_x/SiO_2$ gate oxide interface; and

wherein the $Si_{1-x}Ge_x$ channel region is formed from ion implanting germanium (Ge) into the substrate at a dose of approximately 2 X 10^{16} atoms/cm^2, and wherein the Ge is implanted at an energy of approximately 20 to 100 keV[; and].

[wherein the $Si_{1-x}Ge_x$ channel region has a channel length less than 7μm.]

28. (Five times amended) A p-channel metal-oxide-semiconductor transistor formed on a silicon substrate, comprising:

a $Si_{1-x}Ge_x$ channel region, having a germanium molar fraction of 0.2, and formed in the substrate, underneath [and adjoining] a silicon dioxide (SiO_2) gate oxide and between a source region and a drain region[;], wherein the $Si_{1-x}Ge_x$ channel region forms a $Si_{1-x}Ge_x/SiO_2$ gate oxide interface.

[wherein the $Si_{1-x}Ge_x$ channel region has a channel length less than 7μm.]

32. (Twice amended) The transistor of claim [30] 28, wherein, the [Si-Ge alloy] $Si_{1-x}Ge_x$ channel region was formed by a process comprising:

ion implanting Ge ions through the gate oxide on the substrate at a dose of

approximately 2 X 10^{16} atoms/cm^2, and wherein the Ge was implanted at an energy of approximately 20 to 100 keV; and

annealing the substrate in a furnace at a temperature of approximately 450 to 700 degrees Celsius.

38. (Thrice amended) A [p-channel metal-oxide-]semiconductor transistor, comprising:

a silicon substrate;

a silicon dioxide (SiO_2) gate oxide, coupled to the substrate;

a gate, coupled to the SiO_2 gate oxide;

source/drain regions formed in the substrate on opposite sides of the gate; and

a $Si_{1-x}Ge_x$ channel region, having a germanium molar fraction of x, and located underneath [formed in the substrate, underneath and adjoining] the SiO_2 gate oxide and between the source/drain regions[;], wherein x is less than or equal to 0.6, and wherein the $Si_{1-x}Ge_x$ channel region forms a $Si_{1-x}Ge_x/SiO_2$ gate oxide interface.

[wherein the $Si_{1-x}Ge_x$ channel region has a channel length less than 7μm; and

wherein the germanium molar fraction is less than about 0.6.]

40. (Thrice amended) A [p-channel metal-oxide-]semiconductor transistor formed on a silicon substrate, comprising:

a $Si_{1-x}Ge_x$ channel region, having a germanium molar fraction of [x, and] 0.2 formed in the substrate, underneath [and adjoining] a silicon dioxide (SiO_2) gate oxide and between a source region and a drain region[;], wherein the $Si_{1-x}Ge_x$ channel region forms a $Si_{1-x}Ge_x/SiO_2$ gate oxide interface.

[wherein the $Si_{1-x}Ge_x$ channel region has a channel length less than 7μm; and

wherein the germanium molar fraction is less than about 0.6.]

41. (Twice amended) A semiconductor transistor formed on a silicon substrate, comprising:

a $Si_{1-x}Ge_x$ channel region, having a germanium molar fraction of x, and formed in the substrate, underneath a silicon dioxide (SiO_2) gate oxide and between a source region and a drain region [without a silicon layer interposed between the $Si_{1-x}Ge_x$ channel region and the gate

oxide;], wherein x is less than or equal to 0.6, and wherein the $Si_{1-x}Ge_x$ channel region forms a $Si_{1-x}Ge_x/SiO_2$ gate oxide interface.

wherein the $Si_{1-x}Ge_x$ channel region is formed from ion implanting germanium (Ge) into the substrate at a dose of approximately 2×10^{16} atoms/cm^2, and wherein the Ge is implanted at an energy of approximately 20 to 100 keV[;].

[wherein the germanium molar fraction is less than about 0.6; and

wherein the $Si_{1-x}Ge_x$ channel region has a channel length less than 7μm.]

43. (Once amended) The transistor of claim 41, wherein the Ge is dispersed in the substrate to a depth of approximately 300 angstroms and the germanium molar fraction is [less than] about 0.4.

REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on October 30, 2000, and the references cited therewith.

Claims 11, 24, 25, 28, 32, 38-41, and 43 are amended, claims 30-31 are canceled; as a result, claims 11, 13-14, 24-28, 32, 38-43 are now pending in this application.

§112 Rejection of the Claims

Claims 11, 13, 14, 24-28, 30-32, and 38-40 were rejected under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The limitation cited by the examiner of "a channel length less than 7μm" has been removed from all claims. The Applicant removes this limitation without prejudice or disclaimer, in an effort to move the prosecution forward and Applicant does not concede in Examiner's assertion that this limitation is not enabled by the specification. Withdrawal of Examiner's 35 USC § 112 rejection is therefore respectfully requested.